AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 2, with the following amended paragraph:

The present application is related to U.S. Patent Application "Extended Range Image Processing For Electro-Optical Systems", Serial No. 09/841,079 ~~(Attorney Docket No. 017750-575)~~, and to U.S. Patent Application entitled "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~, both filed even date herewith, the contents of which are hereby incorporated herein by reference in their entirety.

Please replace paragraph [0001] with the following amended paragraph:

The present invention relates to dynamic range compression (DRC) of imagery. An exemplary aspect of the present invention relates to DRC of infrared (IR) imagery and, in particular, to real-time DRC of IR imagery collected with a forward looking infrared (FLIR) camera system.

Please replace paragraph [0002] with the following amended paragraph:

Imagery collected with a large field of view imaging apparatus, such as a wide field of view (WFOV) forward looking infrared (FLIR) pilotage system, may contain low-frequency gradient data, such as ground-to-sky gradient data, that can dominate the dynamic range of the imagery. As a result, ~~Applicants~~ the present inventors have found that detailed scene information can be essentially hidden in a corresponding image displayed on a display device. For example, the ground-to-sky temperature gradient observed by a FLIR system can be 30-40 °C, whereas

neighboring objects on the ground may only exhibit only a 1-2 °C temperature difference. Accordingly, details corresponding to objects on the ground can be difficult or impossible to detect if the low-frequency background gradient is not removed.

Please replace paragraph 0005 with the following amended paragraph:

In another exemplary aspect of the present invention, a method and apparatus for dynamic range compression of image data ~~is provided~~ are provided. The method comprises the steps of down-sampling a frame of image data comprising a first array of pixels to generate a second array of pixels, applying a first median filter to the second array of pixels to generate a blurred array of pixels, up-sampling the blurred array of pixels, and removing at least a portion of low-frequency gradient data generated by previous steps from the frame of image data. In an exemplary aspect, the up-sampling can comprise applying bilinear interpolation. In addition, the first median filter can be a large-area median filter, which can be a sparse large-area median filter. The method can further comprise the steps of applying a second median filter after applying the first median filter, the second median filter having a smaller kernel than the first median filter, and applying a mean filter after applying the second the median filter. The method can further comprise smoothing output data from the mean filter. The apparatus comprises a processor unit coupled to an image-data source, wherein the processor unit can be configured to carry out the above-noted steps.

Please replace paragraph 0025 with the following amended paragraph:

Various aspects of the invention will now be described in connection with a number of exemplary embodiments. To facilitate an understanding of the invention, many aspects of the invention are described in terms of actions to be performed by a processor unit, a processor, and/or one or more field programmable gate array (FPGA) devices. It will be recognized that in each of the embodiments, the various actions could be performed by elements of a computer system. Further, it will be recognized that in each of the embodiments, the various actions could be performed by specialized circuits (e.g., discrete logic gates interconnected to perform a specialized function), by program instructions being executed by one or more processors, or by a combination of both. Moreover, the invention can additionally be considered to be embodied entirely within any form of computer readable carrier such as solid-state memory, magnetic disk, optical disk or modulated carrier wave (such as radio frequency, audio frequency or optical frequency modulated carrier waves) containing an appropriate set of computer instructions that would cause a processor to carry out the techniques described herein. Further, the invention can additionally be considered to be embodied within an appropriate set of computer instructions that can be downloaded via a network connection to cause a processor to carry out the techniques described herein. Thus, the various aspects of the invention can be embodied in many different forms, and all such forms are contemplated to be within the scope of the invention. For each of the various aspects of the invention, any such form of embodiment can be referred to herein as "logic configured to" perform a described action, or alternatively as "logic that" performs a described action.

Please replace paragraph 0026 with the following amended paragraph:

FIG. 1 illustrates a block diagram of an apparatus 100 for gathering and processing imagery, such as infrared (IR) imagery, according to an exemplary aspect of the present invention. The apparatus 100 could, for example, be incorporated into a forward looking infrared (FLIR) camera system such as that described in commonly-assigned U.S. Patent ~~Application No. 09/463,410~~ No. 6,359,681 entitled "Combined Laser/FLIR Optics System", the disclosure of which is hereby incorporated by reference in its entirety.

Please replace paragraph 0028 with the following amended paragraph:

The detector array 102 can be a second generation scanning detector array comprising a plurality of detector channels known to those skilled in the art, and can be configured to collect data corresponding to two-dimensional imagery using appropriate optics (not shown), such as IR optics, and a scanning mechanism (not shown), such as a scanning mirror, also known to those skilled in the art. Additional information pertaining scanning detector arrays can be found, for example, in commonly assigned U.S. Patent Application entitled "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~, incorporated herein by reference as noted above. In addition, if the detector array 102 is a scanning detector array, the apparatus 100 can be configured for two samples per dwell, where dwell refers to the data acquisition time corresponding to a vertical column of image pixels (e.g., for a detector array configured as a column array of detector elements). In other words, the image data

can be over-sampled two-to-one in a horizontal scanning direction. Implications of such over-sampling will be described below. In addition, it should be noted that use of the terms vertical and horizontal is merely for convenience and is not intended to be limiting in any way.

Please replace paragraph 0031 with the following amended paragraph:

The apparatus 100 can also comprise a non-volatile memory 108 and an additional memory 110. The non-volatile memory 108 can be utilized for storing initial values (e.g., factory-calibrated values) of correction coefficients for correcting imagery gathered by the scanning detector array as described in above-incorporated U.S. Patent Application entitled "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~. The additional memory 110 can be utilized, for example, for storing updated values of correction coefficients, such as gain and level coefficients, determined with a scene-based non-uniformity correction (SBNUC) routine, and can also be used for storing image data at various processing levels described below.

Please replace paragraph 0036 with the following amended paragraph:

FIGS. 2 and 3 illustrate functional block diagrams of exemplary FPGA devices 200 and 300 that can be used according to exemplary aspects of the present invention. As shown in FIG. 2, FPGA 200 comprises a processor interface 204, a processor interface bus 208, a memory interface 206, a data input interface 202, and a data output interface 210, and can also comprise an Ethernet controller interface 214 for engineering purposes (e.g., testing) and one or more additional device

interfaces 212 for communicating with and for processing data from other system devices. Moreover, with regard to functional aspects, it can be seen that FPGA 200 can carry out processing related to a power-up correction 218 (utilizing internal coefficient memory 1 220) and processing related to a SBNUC routine 226 (utilizing internal coefficient memory 2 228). In addition, the FPGA 200 can include a SBNUC data collection function 230, which can be a memory location for which both the processor 106A and the FPGA 200 (or 106B) can read and write data for SBNUC processing. An exemplary power-up correction and an exemplary SBNUC routine are disclosed in above-incorporated "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~. In addition, FPGA device 200 can carry out processing related to dead-channel detection 224 and replacement 222, as will be described below. The FPGA device can also carry out test pattern insertion 216 known to those skilled in the art for testing system electronics.

Please replace paragraph 0037 with the following amended paragraph:

In addition, FPGA device 300 illustrated in FIG. 3 similarly comprises a processor interface 304, a processor interface bus 308, a memory interface 306, a data input interface 302, and a data output interface 310. With regard to functional aspects, it can be seen that FPGA device 300 can carry out processing related to extended range processing 314, such as that described in above-incorporated U.S. Patent Application "Extended Range Image Processing For Electro-Optical Systems", Serial No. 09/841,079 ~~(Attorney Docket No. 017750-575)~~. Moreover, FPGA device 300 can also carry out processing related to DRC 316, edge

enhancement 318, noise filtering 320, and display remapping 322 as described in greater detail below. It should be noted that FPGA device 300 can employ a selection box 312 for selectively carrying out processing related to extended range processing or dynamic range (and subsequent) processing. Display remapping refers to adjusting the bit resolution of data for display purposes, for example, converting 12-bit data utilized in computations to 8-bit data appropriate for displaying. Such display remapping is well known in the art and does not need to be described further.

Please replace paragraph 0043 with the following amended paragraph:

FIG. 5 is a block diagram of an exemplary approach 500 for processing image data beginning at step 502. As indicated at step 504, the approach 500 comprises acquiring a frame of image data, such as noted above. As indicated at step 506 in the Example of Figure 5, the approach 500 can optionally further comprise normalizing the frame of image data to generate image data that can be referred to, for example, as second image data or normalized data. This step can be beneficial because image data output from detector arrays utilized in FLIR camera systems, for example, is not expected to be automatically normalized. In an exemplary aspect of the invention, the normalization can comprise correcting the frame of image data using a set of correction coefficients corresponding to detector elements of a detector array used to collect the frame of image data. For example, such correction coefficients can be moment, gain and level coefficients determined for the detector array 102 through a factory calibration using known thermal reference sources. The correction coefficients can additionally be those that have been updated using a

power-up correction to the gain and/or level coefficients. Such exemplary corrections are described in the above-incorporated U.S. Patent Application "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~.

Please replace paragraph 0044 with the following amended paragraph:

In addition, as noted at step 508, in the example of Figure 5, the approach 500 can also optionally comprise applying a dead-channel-replacement correction to generate image data that can be referred to, for example, as third image data or dead-channel-corrected data. The procedure for dead-channel replacement is known in the art, and is described, for example, in the above-incorporated U.S. Patent Application No. 09/463,410 and also in the above-incorporated U.S. Patent Application "Extended Range Image Processing For Electro-Optical Systems", Serial No. 09/841,079 ~~(Attorney Docket No. 017750-575).~~

Please replace paragraph 0045 with the following amended paragraph:

In addition, as noted at step 510 in the example of Figure 5, the approach 500 can also optionally comprise applying a scene-based non-uniformity correction (SBNUC) to the third image data to generate fourth image data (e.g., SBNUC-corrected data). An exemplary SBNUC routine applicable to scanning detector arrays is described in the above-incorporated U.S. Patent Application "Scene-Based Non-Uniformity Correction For Detector Arrays", Serial No. 09/840,920 ~~(Attorney Docket No. 017750-604)~~. Other SBNUC methods applicable to two-dimensional detector arrays are described, for example, in U.S. Patent No. 5,721,427 "Scene-

Based Nonuniformity Correction Processor Incorporating Motion Triggering", U.S. Patent No. 5,925,880 "Non Uniformity Compensation for Infrared Detector Arrays", U.S. Patent No. 5,903,659 "Adaptive Non-Uniformity Compensation Algorithm", and U.S. Patent No. 6,018,162 "System With Motion Detection Scene-Based Non-Uniformity Correction", the disclosures of which are hereby incorporated by reference in their entirety.

Please replace paragraph 0059 with the following amended paragraph:

Exemplary LAMFs with 7 x 7 kernel sizes and having active elements arranged in predetermined patterns are illustrated in FIGS. 8A and 8B. A 7 x 7 kernel size has been used, for example, with a 16 x 32 down-sampling filter, providing an effective area of 112 x 224 pixels over which the LAMF is applied. According to one exemplary aspect of the present invention, the predetermined pattern can be configured as a star-shaped pattern, such as illustrated in FIG. 8A. Alternatively, the predetermined pattern can be configured as a checkerboard pattern, such as illustrated in FIG. 8B. In addition, various other patterns can also be utilized, and the ~~pattens~~ patterns shown in FIGS. 8A and 8B are not intended to be restrictive. In each of these exemplary patterns, the number of active elements is 25, whereas the total number of elements in the kernel is 49. It should be noted that where computational efficiency is not of primary importance, it can be advantageous to apply a LAMF where all elements of the kernel are active elements. However, where it is important to consider hardware constraints and the associated effects on computational efficiency, it can be advantageous to utilize sparse LAMFs, such as those illustrated in FIGS. 8A and 8B. Other kernel sizes for the LAMF can also be

used. For example, a kernel size of 13 x 13 has been used with a 8 x 16 down-sampling filter, providing an effective area of 104 x 208 pixels over which the LAMF is applied. An exemplary 13 x 13 LAMF in a star-shaped pattern is illustrated in Figure 8C. Of course, checker-board or other patterns could also be utilized.

Please replace paragraph 0068 with the following amended paragraph:

As indicated at step 712, the approach 700 further comprises applying up-sampling to the blurred array of pixels to generate up-sampled data. Up-sampling generates low-frequency gradient data information that can then be removed from the frame of image data input to the DRC algorithm. In an exemplary aspect of the present invention, this up-sampling can comprise applying bilinear interpolation (BLI) and can also be referred to as a BLI zoom. BLI is well known in the art, and exemplary BLI is described in U.S. Patent No. 5,801,678 "Fast Bi-Linear Interpolation Pipeline", the disclosure of which is hereby incorporated by reference in its entirety, and in above-incorporated U.S. Patent Application "Extended Range Image Processing For Electro-Optical Systems", Serial No. 09/841,079 ~~(Attorney Docket No. 017750-575)~~.